SPECIFICATION

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[LITHOGRAPHY PROCESS]

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to a lithography process, and more particularly, to a universal lithography re-work process.

[0003] 2. Description of the Prior Art

[0004] Semiconductor chips are manufactured by executing at least tens of lithography processes. To execute a lithography process, the surface of the semiconductor chip is covered with a photoresist layer, and an exposure process is performed using a photomask to project mask patterns onto the photoresist layer. The chemical property of the photoresist layer after exposure is thus changed and a developer is utilized to remove the exposed photoresist or the unexposed photoresist to form the layout patterns corresponding to the mask in the photoresist layer. The residual photoresist layer is removed after some corresponding semiconductor processes to form the expected layout patterns on the semiconductor chip.

[0005] With the rapid development of semiconductor processing, the line width has shrunk and the number of masks used is continuously increasing. An accurate lithography process is the key to the remarkable processing ability of a semiconductor manufacturer. The quality of the lithography process depends on the accuracy of the exposure process. Errors during the exposure process can cause the mask patterns to be formed in incorrect locations causing the layout patterns within different layers not to be connected properly. An open circuit or a circuit with poor conductivity is the most common occurrence. To avoid this type of manufacturing defect , alignment marks are formed on the mask so corresponding alignment marks are formed in the photoresist layer after the exposing and developing processes. An after development

inspection (ADI) process is thereafter executed by precise instruments to ensure the correctness of the lithography process. Any abnormal wafer is discovered at this stage and is sent to a rework process rather than going to subsequent processes.

[0006] Please refer to Fig. 1 and Fig. 2. Fig. 1 is a schematic diagram of performing a lithography process and a rework process on a semiconductor wafer 60 according to the prior art. Fig. 2 is a flowchart 20 of a lithography process and a rework process according to the prior art. As shown in Fig.1 and Fig.2, the method for executing a lithography process and a rework process according to the prior art includes the following steps. First, at least one semiconductor wafer 60 is provided (step 30). A silicon substrate 61 is comprised on a surface of the semiconductor wafer 60. At least one deposition layer 62 is comprised on a surface of the silicon substrate 61. The deposition layer 62, being a thin film frequently used in semiconductor process, comprises a silicon dioxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer, a silicon oxynitride (SiO_xN_y) layer, a polysilicon layer, or a metal layer.

[0007] Then a standard lithography process is performed on the semiconductor wafer 60 (step 32). If the deposition layer 62 is not comprised on the surface of the silicon substrate 61, a patterned photoresist layer 64 formed by the lithography process is used for defining the layout pattern of an ion implantation area or a shallow trench isolation (STI) on the surface of the silicon substrate 61. If the deposition layer 62 is comprised on the surface of the silicon substrate 61, a patterned photoresist layer 64 formed by the lithography process is used for defining the layout pattern of the deposition layer 62. In Fig.1, the silicon substrate 61 comprising the deposition layer 62 is an example. The layout pattern comprises the pattern of a gate, a via plug, a contact plug, a dual damascence structure, a top plate of a capacitor, a bottom plate of a capacitor, a node contact, a word line, a bit line, a metal line, or a bonding pad depending on the material composition of the deposition layer 62 and the process stage.

[0008]

It is worth noticing that an anti-reflection coating 66 (ARC) is disposed underneath the bottom of the patterned photoresist layer 64, underneath the bottom of the deposition layer 62, or both. The anti-reflection coating 66 is substantially composed of titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), or silicon

oxynitride, depending on the material composition of the deposition layer 62 and the process requirement. The anti-reflection coating 66 is used for preventing reflections from the surface of the deposition layer 62 during exposure. Hence, the accuracy of the patterned photoresist layer 64 is not decreased.

[0009] An after development inspection (ADI) process is thereafter performed (the first ADI process, step 34). The ADI process, being a quality control step, utilizes precise optical equipment and alignment marks (not shown) on the semiconductor wafer 60 to ensure the correctness of the patterned photoresist layer 64, such as the spec for the thickness of the developed photoresist layer, the shape of the patterns, the relative sites, and the sizes of the patterns. If the semiconductor wafer 60 fulfills the spec, a hard bake process is performed to reduce the content of the residue solvent in the photoresist layer as low as possible by evaporation. The standard lithography process (step 32) is thus completed and the next process step is performed (step 42). The next process step could be an etching process or an ion implantation process.

[0010] If the semiconductor wafer 60 is out of spec, a plasma ash strip process, utilizing plasma and reactive etching, is performed (step 36) to remove the incorrect patterned photoresist layer 64. After that, a cleaning and rinsing process is performed (step 38) to remove the ash-formed photoresist layer, the polymer residue, particles, and metal contamination remaining on the surface of the semiconductor wafer 60. A fluorine based solvent, an amine based solvent, or at least one chemical is first utilized to perform a wet cleaning process. A rinsing process and a drying process are thereafter performed.

[0011] An inspection process after cleaning is performed (step 40) to ensure the cleanness of the semiconductor wafer 60. In a semiconductor production line, the specs for various products and various process stages are established. Therefore when the size and the quantity of the photoresist layer, the polymer residue, particles, metal contamination, and the micro roughness remaining on the surface of the semiconductor wafer 60 fulfill the spec, the cleaning and rinsing process is completed and the semiconductor wafer 60 is sent back to the standard lithography process (step 32).

[0012] Similarly to a new wafer, an ADI process is performed on a reworked wafer after

the patterned photoresist layer 64 is reformed (the ADI process, step 34, performed a second time) to ensure the correctness of the patterned photoresist layer 64. If the semiconductor wafer 60 fulfills the spec, the subsequent processes are performed as described before. If the semiconductor wafer 60 does not fulfill the spec, the semiconductor wafer 60 is sent back to the plasma ash strip process step (step 36). The photoresist is removed again by utilizing plasma and reactive etching. After that, the subsequent processes are performed as described before.

[0013] The plasma ash strip process (step 36), the cleaning and rinsing process (step 38), the inspection process after cleaning (step 40), the standard lithography process (step 32), and the second ADI process (step 34) is the whole of the rework process.

[0014] The flowchart 20 of a lithography process and a rework process according to the prior art comprises the following steps:

[0015] Step 30:Provide at least one semiconductor wafer;

[0016] Step 32:Perform a standard lithography process to the semiconductor wafer;

[0017] Step 34:Perform an ADI process, if the semiconductor wafer fulfills the spec, go to step42; if the semiconductor wafer does not fulfill the spec, go to step 36;

[0018] Step 36:Perform a plasma ash strip process;

[0019] Step 38:Perform a cleaning and rinsing process;

[0020] Step 40:Perform an inspection process after cleaning, if the semiconductor wafer fulfills the spec, go to step 32; if the semiconductor wafer does not fulfill the spec, go to step 36; and

[0021] Step 42:Perform the next process step.

[0022] The incorrectly patterned photoresist layer is removed and a correct patterned photoresist layer is reformed with the addition of several processing steps by executing the lithography process and the rework process according to the prior art. Problems, such as junction leakage current lifting, bridge, decreased yield, decreased oxide breakdown voltage, and change of threshold voltage of a metal-oxide semiconductor, are also avoided due to sufficient cleanness of the surface of the

semiconductor wafer. However, with the consideration of forming a correct patterned photoresist layer and ensuring the cleanness, it is frequently observed that the surface of the semiconductor wafer is changed or damaged after the plasma ash strip process and the cleaning and rinsing process. The poor photoresist adhesion problem during a subsequent lithography process, the profile change problem, and the fall down problem occur this way making a rework process difficult or unfeasible.

Summary of Invention

[0023] It is therefore a primary objective of the claimed invention to provide a lithography process and method to resolve the above-mentioned problem, and to reduce the quantity of the scrap semiconductor wafers due to a rework process.

[0024] According to the claimed invention, a substrate is provided first. Then a protective layer is formed on a surface of the substrate. A patterned photoresist layer is thereafter formed on a surface of the protective layer. Finally, a first inspection process is performed to screen the correctness of the patterned photoresist layer. When the correctness of the patterned photoresist layer fulfills the spec, a normal process is performed to the substrate. When the correctness of the patterned photoresist layer does not fulfill the spec, the patterned photoresist layer on the surface of the protective layer is removed and the patterned photoresist layer is reformed on the surface of the protective layer by a rework process.

[0025] It is an advantage of the claimed invention to perform a lithography process and a rework process by forming a very thin protective layer on the surface of the semiconductor wafer, which will not disturb the subsequent etching process and ion implantation process, then perform the lithography process. When the correctness of the patterned photoresist layer does not fulfill the spec, the rework process for reforming a correct patterned photoresist layer does not affect the cleanness and the quality of the surface of the semiconductor wafer. When the correctness of the patterned photoresist layer fulfills the spec, the very thin protective layer does not affect subsequent normal processing. In summary, the production yield is raised and the quantity of scrap wafers incurred from the rework process is reduced when applying the claimed invention method to the production line.

[0026] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment, which is illustrated in the various figures and drawings.

Brief Description of Drawings

[0027] Fig. 1 is a schematic diagram of performing a lithography process and a rework process on a semiconductor wafer according to the prior art.

[0028] Fig. 2 is a flowchart of a lithography process and a rework process according to the prior art.

[0029] Fig. 3 is a schematic diagram of performing a lithography process and a rework process on a semiconductor wafer according to the present invention.

[0030] Fig. 4 is a flowchart of a lithography process and a rework process according to the present invention.

Detailed Description

[0031] Please refer to Fig.3 and Fig.4. Fig.3 is a schematic diagram of performing a lithography process and a rework process on a semiconductor wafer 160 according to the present invention. Fig.4 is a flowchart 120 of a lithography process and a rework process according to the present invention. As shown in Fig.3 and Fig.4, the method for executing a lithography process and a rework process according to the present invention includes the following steps. Firstly at least one semiconductor wafer 160 is provided (step 130). A silicon substrate 161 is comprised on a surface of the semiconductor wafer 160. At least one deposition layer 162 is further comprised on a surface of the silicon substrate 161. The deposition layer 162, being a thin film frequently used in semiconductor process, comprises a silicon dioxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer, a silicon oxynitride (SiO_xN_y) layer, a polysilicon or a metal layer.

[0032] Then a protective layer 164 is formed on the surface of the semiconductor wafer 160 (step 132). The protective layer 164 is a silicon oxide layer, a tetra-ethyl-ortho-silicate (TEOS) layer, or other dielectric layer having a thickness of approximately 50 Å . If the protective layer 164 is a silicon oxide layer or a tetra-ethyl-ortho-silicate

layer, the protective layer 164 is formed by a low pressure chemical vapor deposition (LPCVD) process or a plasma enhanced chemical vapor deposition (PECVD) process. When considering the material composition of the protective layer 164, it is necessary that the surface property of the protective layer 164 will not change during a plasma ash strip process or a cleaning and rinsing process. In addition, the thickness of the protective layer 164 needs to be very thin so the subsequent etching and ion implantation processes are not disturbed.

[0033] A standard lithography process is performed to the semiconductor wafer 160 (step 134). If the deposition layer is not comprised on the surface of the silicon substrate 161, a patterned photoresist layer 166 formed by the lithography process is used for defining the layout pattern of an ion implantation area or a shallow trench isolation (STI) on the surface of the silicon substrate 161. If the deposition layer 162 is comprised on the surface of the silicon substrate 161, a patterned photoresist layer 166 formed by the lithography process is used for defining the layout pattern of the deposition layer 162.

[0034] In Fig.3, the silicon substrate 161 comprising the deposition layer 162 is an example. The layout pattern comprises the pattern of a gate, a via plug, a contact plug, a dual damascence structure, a top plate of a capacitor, a bottom plate of a capacitor, a node contact, a word line, a bit line, a metal line, or a bonding pad depending on the material composition of the deposition layer 162 and the process objective.

[0035] It is worth noticing that an anti-reflection coating 168 is disposed underneath the bottom of the patterned photoresist layer 166, underneath the bottom of the deposition layer 162, or both. The anti-reflection coating 168 is substantially composed of titanium (Ti), titanium nitride (TiN), titanium tungsten (TiW), or silicon oxynitride depending on the material composition of the deposition layer 162 and the process requirement. The anti-reflection coating 168 is used for preventing reflections from the surface of the deposition layer 162 during exposure. Hence, the accuracy for the patterned photoresist layer 166 is not decreased.

[0036] An after development inspection (ADI) process is thereafter performed (the first ADI process, step 136). The ADI process, being a quality control step, utilizes precise

optical equipment and alignment marks (not shown) on the semiconductor wafer 160 so as to ensure the correctness of the patterned photoresist layer 166, such as the spec for the thickness of the developed photoresist layer, the shape of the patterns, the relative sites, and the sizes of the patterns. If the semiconductor wafer 160 fulfills the spec, a hard bake process is performed to reduce the content of the residue solvent in the photoresist layer as low as possible by evaporation. The standard lithography process (step 134) is thus completed and the next process step is performed(step 144). The next process step could be an etching process or an ion implantation process. Since the protective layer 164 is very thin, the subsequent etching process or ion implantation process is not disturbed. The protective layer 164 may be or may not be removed after completing the next process step, depending on the device structure, the device category, and the process requirement.

[0037] If the semiconductor wafer 160 is out of spec, a plasma ash strip process, utilizing plasma and reactive etching, is performed (step 138) to remove the incorrect patterned photoresist layer 166. After that, a cleaning and rinsing process is performed (step 140) to remove the ash-formed photoresist layer, the polymer residue, particles, and metal contamination remaining on the surface of the semiconductor wafer 160. A fluorine based solvent, an amine based solvent, or at least one chemical is first utilized to perform a wet cleaning process. A rinsing process and a drying process are thereafter performed. Since the material composition of the protective layer 164 is compatible with the plasma ash strip process and the cleaning and rinsing process, the surface property of the protective layer 164 will not change during these processes. Hence, the protective layer 164 is able to protect the surface of the semiconductor wafer 160 from problems such as poor photoresist adhesion during a subsequent lithography process, a profile change, and fall down.

[0038] An inspection process after cleaning is performed (step 142) to ensure the cleanness of the semiconductor wafer 160. In semiconductor production line, the specs for various products and various process stages are established. Therefore, when the size and the quantity of the photoresist layer, the polymer residue, particles, metal contamination, and the micro roughness remaining on the surface of the semiconductor wafer 160 fulfill the spec, the cleaning and rinsing process is completed and the semiconductor wafer 160 is sent back to the standard lithography

process (step 134).

[0039] An ADI process is performed after the patterned photoresist layer 166 is reformed (the ADI process, step 136, performed a second time) to ensure the correctness of the patterned photoresist layer 166. After that, the subsequent processes are performed as described before. If the semiconductor wafer 160 does not fulfill the spec, the semiconductor wafer 160 is sent back to the plasma ash strip process step (step 138). The photoresist layer 166 is removed again by utilizing plasma and reactive etching. Next, the subsequent processes are performed as described before.

[0040] The plasma ash strip process (step 138), the cleaning and rinsing process (step 140), the inspection process after cleaning (step 142), the standard lithography process (step 144), and the second ADI process (step 136) is the whole of the rework process.

[0041] The flowchart 120 of a lithography process and a rework process according to the present invention comprises the following steps:

[0042] Step 130:Provide at least one semiconductor wafer;

[0043] Step 132:Form a protective layer on the surface of the semiconductor wafer;

[0044] Step 134:Perform a standard lithography process to the semiconductor wafer;

[0045] Step 136:Perform an ADI process, if the semiconductor wafer fulfills the spec, go to step 144; if the semiconductor wafer does not fulfill the spec, go to step 138;

[0046] Step 138:Perform a plasma ash strip process;

[0047] Step 140:Perform a cleaning and rinsing process;

[0048] Step 142:Perform an inspection process after cleaning, if the semiconductor wafer fulfills the spec, go to step 134; if the semiconductor wafer does not fulfill the spec, go to step 138; and

[0049] Step 144:Perform the next process step.

[0050] The method of performing a lithography process and a rework process according to the present invention is to form a very thin protective layer, which will not disturb

the subsequent etching process and ion implantation process, on the surface of the semiconductor wafer, then perform the lithography process. When the correctness of the patterned photoresist layer does not fulfill the spec, the rework process for reforming a correct patterned photoresist layer does not affect the cleanness and the quality of the surface of the semiconductor wafer. When the correctness of the patterned photoresist layer fulfills the spec, the very thin protective layer does not affect the subsequent normal processes.

[0051] In contrast to the prior art method of performing a lithography process and a rework process, the present invention method is to form a very thin protective layer on the surface of the semiconductor wafer, then perform the lithography process and the rework process. Since the protective layer is very thin, it will not disturb the subsequent etching process or ion implantation process. Under this premise, a correct patterned photoresist layer is reformed with the addition of several process steps and the surface of the semiconductor wafer sufficiently clean. In addition, the surface condition of the protective layer does not change due to the plasma ash strip process and the cleaning and rinsing process. The protective layer therefore effectively protects the surface structure of the semiconductor wafer to avoid the poor photoresist adhesion problem during subsequent lithography process, the profile change problem, and the fall down problem. The feasibility for rework process is greatly enhanced. In summary, the production yield is raised and the quantity of scrap wafers incurred from rework process is reduced when applying the present invention method to the production line.

[0052] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.